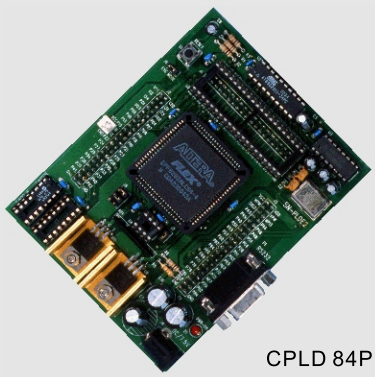
CIC-310

CPLD/FPGA Digital Circuits Development System

- The laptop shown in the picture is not a product of CIC-310. It is for demonstration purpose only.
- The appearance of the product may be changed due to the new version release.



CPLD 84PIN

Contents of the Product

1. FPGA (8000/8K) download board (84pin)
2. I/O experiments board
3. MAX+PLUS® II development software (student version)
4. Program manager software for program download and In-System-Programming
5. Experiment manual

Features of the Download Board

1. The FPGA has more than 2500/10000 gate counts. The SRAM based interior cells enables the chip to reach several hundred MHz operating speed
2. On the basis of ISP architecture, it's free from buying extra burning devices. Users can download the program to either SEEPROM or FPGA chip through RS-232 interface.
3. Users can move several programs to the download board with the function of on-board SEEPROM and program manager interface. After download, only jumper is needed to select the program.
4. Data compression function allows users to save more programs in the SEEPROM (above ten thousand times).
5. 64Kbit SEEPROM can be upgrade to 256Kbit
6. All of the pins of the I/O components are assigned to certain pins of the FPGA chip. Users only have to focus on the FPGA pin assignments in MAX+PLUS® II after programming.
7. The download board can be replaced by other FPGA chip (Altera EPF-8000/10K) upon request.

Specifications of Experiment Board

1. Signal Generator : Two sets of continuous adjustable signal generators generating 0.1Hz~500KHz pulse signal
2. Pulse Generator : 4 sets of pulse generator with the implementation of the debounce circuit
3. Input Switch : 3 sets of 8 bit logic input DIP switches Only 2 sets are monitored by 16 LEDs
4. Output LED display: 32 LEDs display with digital buffer output
5. Matrix Keypad: 4x4 matrix keypad can be set to 16 independent push-button switches or 3x4 matri x keypad and 4 push-button switches
6. Quartz OSC Signal: Two sets of oscillation frequency are available for selection (20MHz, 11.059MHz). 20MHz OSC with socket could easily change the oscillator.
7. 7-Segment LED Display: 6 digits of 7-segment display which can be set to either parallel or serial scan.
8. Alpha-Numeric LED Display: 16-segment LED drives the display
9. 5x7 Dot Display: 5x7 dot matrix drives the display

List of the Experiments

1. Designing combinational logic circuit
2. Designing sequential logic circuit
3. Designing flip-flops circuit
4. Designing counters and applications
5. Designing ALUs and applications
6. Designing encoder/decoder and multipliers/demultipliers
7. Designing frequency synthesizer and shift registers
8. Production and application of digital circuit

The MAX+PLUS® II development software provides a complete design environment that easily adapts to your specific design needs.

Simplify, Clarify, and Verify

Behavioral model with a hardware description language (HDL) is the key to modern logic design courses. Today, most engineers use an HDL-based design method to create a high-level, language-based, abstract description of a circuit, synthesize a hardware circuits in a CPLD or FPGA technology, and verify its functionality and timing.

This product serves to build up students' understanding in logic design courses by (1) reviewing basic principles of combinational and sequential logic, (2) introducing the use of HDLs in design, (3) emphasizing descriptive styles that will allow user to quickly design working circuits suitable for CPLD or FPGA implementation, and (4) providing in-depth design examples using modern design tools MAX+PLUS®II. Students will be encouraged to simplify, clarify, and verify their designs.

Design flow chart